

## IN THE CLAIMS

1. (Original) A semiconductor die comprising:
  - a test signal redistribution layer comprising conductive traces;
  - a test probe point for accessing signals in said semiconductor die and for electrical coupling to said test signal redistribution layer; and
  - a conductive bump for transmitting said signals off of said semiconductor die, said conductive bump located on a first surface of said semiconductor die and electrically coupled to said test signal redistribution layer.
2. (Original) The semiconductor die of Claim 1 wherein said semiconductor die is a flip chip die configured for connection to a package substrate such that said conductive bump is electrically coupled to a test signal access component of said package substrate.
3. (Original) The semiconductor die of Claim 1 wherein said test probe point is accessible by drilling from said first surface of said semiconductor die.
4. (Original) The semiconductor die of Claim 1 wherein said test probe point comprises a focused ion beam (FIB) pad accessible by focused ion beam drilling and conductive material backfill.
5. (Original) The semiconductor die of Claim 4 wherein said FIB pad is a coupled to said test signal redistribution layer by said conductive material backfill.

6. (Original) The semiconductor die of Claim 1 wherein said conductive traces are disposed such that multiple test signals are accessible at varying degrees of electronic component granularity.

7. (Original) The semiconductor die of Claim 1 wherein said conductive traces are routed in a spiral pattern with conductive fingers located in positions such that drilling and conductive material backfill to lower components provides access to varying degrees of signals between components of said semiconductor die.

8. (Withdrawn) A semiconductor fabrication method:  
forming electronic circuits on said semiconductor die;  
forming a test pad in said semiconductor die for access by drilling and conductive material backfill;  
depositing a test signal redistribution layer comprising conductive traces on said semiconductor die; and  
fabricating a conductive bump for conveying a signal to an external access point on a package substrate, said conductive bump located on a first surface of said semiconductor die and electrically coupled to said test signal redistribution layer.

9. (Withdrawn) The method of Claim 8 wherein said semiconductor die is a flip chip die configured for connection to said package substrate such that said conductive bump is electrically coupled to a test signal access component of said

package substrate, said test signal access component coupled to said external access point.

10. (Withdrawn) The method of Claim 8 wherein said conductive traces are disposed such that multiple test signals are accessible at varying degrees of electronic component granularity.

11. (Withdrawn) The method as recited in Claim 8 further comprising accessing said signal at said external access point.

12. (Withdrawn) The method as recited in Claim 8 wherein said fabricating said test signal redistribution layer comprises:

fabricating a said conductive traces in a spiral pattern; and  
fabricating a plurality of conductive fingers extending from said conductive traces, such that a larger area of said semiconductor die is accessed.

13. (Original) A semiconductor device comprising:  
a package substrate for communicating test signals on an external access point; and  
a semiconductor die having test probe points accessible by said external access point, wherein said semiconductor die is electrically coupled to said package substrate.

14. (Original) The semiconductor device of Claim 13 wherein said package substrate comprises:

a first surface with ball grid array;

a second surface with conductive contacts for electrically coupling with conductive bumps of said semiconductor die; and

a trace for electrically coupling one of said conductive contacts to said external access point.

15. (Original) The semiconductor device of Claim 13 wherein said semiconductor die comprises:

a test signal redistribution layer comprising conductive traces;

a test probe point for accessing signals in said semiconductor die and for electrical coupling to said test signal redistribution layer;

a test access via for electrically coupling said test probe point to said test signal redistribution layer; and

a conductive bump for conveying a test signal off of said semiconductor die to said package substrate, said conductive bump located on a first surface of said semiconductor die and electrically coupled to said test signal redistribution layer.

16. (Original) The semiconductor device of Claim 15 wherein said probe point comprises a focused ion beam (FIB) pad accessible by focused ion beam drilling and conductive material backfill.

17. (Original) The semiconductor device of Claim 15 wherein routing of said test signal redistribution layer conductive traces is such that trace widths and spacing is a minimum without causing signal interference.

18. (Original) The semiconductor device of Claim 14 wherein said external access point is accessible by automatic test equipment.

19. (Withdrawn) A semiconductor test process comprising:  
determining a boring location aligned to a test signal redistribution layer and a probe point in a semiconductor die;  
boring a hole to said probe point in a first surface of said semiconductor die;  
backfilling said hole with conductive material to couple said test signal redistribution layer and said probe point;  
coupling electrically a conductive bump on said first surface of said semiconductor die to a conductive component of a second surface of said package substrate, wherein said conductive bump is electrically coupled to said test signal redistribution layer; and  
measuring test signals at an external access point of said package substrate.

20. (Withdrawn) The process of claim 18 wherein said probe point is electrically coupled to a particular signal trace in said semiconductor die.

21. (Withdrawn) The process of claim 18 wherein said test signal is an internal semiconductor die signal while said semiconductor die is operating.

22. (Withdrawn) The process of claim 18 wherein said measuring is performed by automatic test equipment.

23. (Withdrawn) The process of claim 18 wherein said test signal redistribution layer comprises a plurality of conductive traces routed in a spiral pattern.

24. (Withdrawn) The process of claim 23 wherein said test signal redistribution layer further comprises a plurality of conductive fingers extending from said plurality of conductive traces, such that a larger area of said semiconductor die is accessed.

25. (Withdrawn) The process of claim 18 wherein said boring and said backfilling are performed using a focused ion beam (FIB).